

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	Group Art Unit:	<i>Unassigned</i>
Sujatha Kashyap	§		
	§		
Serial No.: <i>Unassigned</i>	§	Examiner:	<i>Unassigned</i>
	§		
Filing Date: <i>Herewith</i>	§		
	§		
Title: Memory Mapping To Reduce Cache Conflicts In Multiprocessor Systems §	§	Docket No.:	AUS920030955US1

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Submitted herewith are patents, publications or other information of which the undersigned is aware, which she believes may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with CFR 1.97(b) the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits. 37 CFR 1.97(b).

A list of the patents(s) and/or publications(s) is set forth on the attached Form PTO/SB/08a & b.

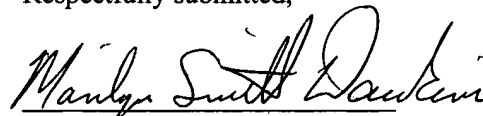
A concise explanation of the items listed on PTO/SB/08a is not given.

The person making this statement is the attorney who signs below on the basis of the information in the attorney's file.

Respectfully submitted,

Date: Feb. 12, 2004

By:



Marilyn Smith Dawkins
Reg. No. 31,140
Intellectual Property Law Dept.
IBM Corporation
11400 Burnet Road 4054
Austin, Texas 75758
Telephone: (512) 823-0094

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Complete if Known

Application Number

Filing Date

Herewith

First Named Inventor

Suiatha Kashvap

Art Unit

Examiner Name

Attorney Docket Number

AUS920030955US1

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ ~Number ⁴ ~Kind Code ⁵ (if known)	MM-DD-YYYY			
	B1	JP 2002342163 A	11-29-2002	Fujitsu LTD		
	B2	JP 2001282547 A	10-12-2001	NEC Microsystem		
	B3	JP 2001216140 A	08-10-2001	NEC Microsystem		

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Application Number

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Herewith

First Named Inventor

Sujatha Kashyap

Art Unit

Examiner Name

Attorney Docket Number

AUS920030955US1

Sheet

2

of

2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C1	JIAN HUANG, et al.; Page-Mapping Techniques for CC-NUMA Multiprocessors; 1997; pp 91-104; (0-7803-4229-1/97 1997 IEEE); US	
	C2	RUI MIN, et al., Improving Performance of Large Physically Indexed Caches by Decoupling Memory Addresses from Cache Addresses, Nov. 2001, Vol 50, No 11; IEEE Transactions; US	
	C3	JACK L. LO, et al.; An Analysis of Database Workload Performance on Simultaneous Multithreaded Processors; US	
	C4	R. E. KESSLER et al.; Page Placement Algorithms for Large Real-Indexed Caches; Nov. 1992; pp 338-359; Vol 10, No 4; ACM Transactions on Computer Systems; US	
	C5	JOCHEN LIEDTKE; Colorable Memory; 11/10/96; pp 1-4; IBM; US	

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